CLAIM AMENDMENTS

In the Claims:

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. (Previously Presented) A method for manufacturing a PIN diode, comprising the following steps:

forming a p-area on a first surface of a wafer;

forming an n-area on the first surface of the wafer spaced apart from the p-area;

forming an intermediate area on the first surface of the wafer between the p-area and the n-area, wherein a doping concentration of the intermediate area is lower than a doping concentration of the p-area and lower than a doping concentration of the n-area;

forming a first electrically conductive member on a side of the p-area, which faces away from the intermediate area; and

forming a second electrically conductive member on a side of the n-area, which faces away from the intermediate area.

2. (Previously Presented) The method in accordance with claim 1, comprising the following steps:

providing the wafer and a device wafer; and

wafer-bonding of the wafer and the device wafer, wherein the p-area, the n-area and the intermediate area are formed in the device wafer and insulated against the wafer.

3. (Previously Presented) The method in accordance with claim 2, comprising the following steps:

forming a trench in a section of the device wafer, which abuts on the intermediate area, wherein the trench extends from a surface of the device wafer, which faces away from the wafer, to a surface of the device wafer, which is opposite to the wafer; and

filling the trench with an insulating material.

4. (Previously Presented) The method in accordance with claim 3, wherein the trench is further formed in sections of the device wafer, which abut on the p-area and on the n-area.

5. (Previously Presented) The method in accordance with claim 2, wherein the p-area or the n-area, respectively, is formed by

forming a trench in the device wafer and filling the same with p-doped or n-doped polysilicon, respectively, or by

implanting of p-material or n-material, respectively, in predetermined areas of the device wafer, or by

forming a trench in the device wafer, introducing of p-material or n-material, respectively, into the same and diffusing of the introduced material into the areas of the device wafer surrounding the trench.

6. (Previously Presented) The method in accordance with claim 1, further comprising the following step:

forming an insulating layer above the surface of the p-area, the n-area, and the intermediate area, which faces away from the first surface of the wafer.

7. (Withdrawn) The method in accordance with claim 1, further comprising the following step:

forming of pads on the surfaces of the p-area and the n-area, which face away from the first surface of the wafer.

8. (Previously Presented) A PIN diode comprising:

a p-area on a first surface of a wafer;

an n-area on the first surface of the wafer;

an intermediate area on the first surface of the wafer between the p-area and the n-area, wherein a doping concentration of the intermediate area is lower than a doping concentration of the p-area and lower than a doping concentration of the n-area;

a first electrically conductive member, which is arranged on a side of the p-area, which faces away from an intermediate area; and

a second electrically conductive member, which is arranged on a side of the n-area, which faces away from the intermediate area.

9. (Previously Presented) The PIN diode in accordance with claim 8, having an insulating layer on the wafer and a device wafer on the insulating layer, wherein the p-area, the n-area, and the intermediate area are arranged in the device wafer.

10. (Previously Presented) The PIN diode in accordance with claim 8, comprising:

a trench in a section of the device wafer, which abuts on the intermediate area, wherein the trench extends from a surface of the device wafer, which faces away from the wafer, to a surface of the device wafer, which is opposite to the wafer, and wherein the trench is filled with an insulating material.

11. (Previously Presented) The PIN diode in accordance with claim 10, wherein the trench is arranged in sections of the device wafer, which abut on the p-area and on the n-area.

12. (Original) The PIN diode in accordance with claim 11, wherein a shape of the intermediate area, which is determined by the trench, is essentially rectangular, wherein the p-area and the n-area are arranged on two opposite sides of the intermediate area.

13. (Canceled)

14. (Original) The PIN diode in accordance with claim 12, wherein at least either the p-area or the n-area extend along a whole width of the intermediate area.

15. (Withdrawn) The PIN diode in accordance with claim 11, wherein a shape of the intermediate area, which is determined by the trench is essentially trapezoidal, wherein the p-area extends along one of the parallel sides of the intermediate area, and wherein the n-area extends along the other of the parallel sides of the intermediate area.

16. (Withdrawn) The PIN diode in accordance with claim 11, wherein a shape of the intermediate area, which is determined by the trench, is essentially circular, wherein either the p-area or the n-area is arranged in the shape of a circle along the edge of the intermediate area, wherein the n-area or the p-area, respectively, is essentially arranged in the

center of the intermediate area and wherein the second electrically conductive member or the first electrically conductive member, respectively, is arranged in its center.

17. (Previously Presented) The PIN diode in accordance with claim 8, further comprising:

a further insulating layer, which covers surfaces of the p-area, the n-area, and the intermediate area, which face away from the wafer.

18. (Withdrawn) The PIN diode in accordance with claim 8, wherein a first pad is conductively connected to the p-area and a second pad is conductively connected to the n-area, wherein the two pads are arranged at the surfaces of the p-area and the n-area, which face away from the first surface of the wafer.

19. (Original) The PIN diode in accordance with claim 8, wherein the distance between the p-area and the n-area is more than 30 μm.

20. (New) The PIN diode in accordance with Claim 8, further comprising first and second pads, said first pad is electrically connected to a surface of the p-area, said second pad is electrically connected to a surface of the n-area, wherein said surfaces face away from the first surface of the wafer.